

1 **WHAT IS CLAIMED IS**

1 1. A method of checking overlap accuracy of patterns on
2 four stacked semiconductor layers, comprising:

3 forming a first checking pattern on a first semiconductor
4 layer, a second checking pattern on a second semiconductor
5 layer, a third checking pattern on a third semiconductor
6 layer and a fourth checking pattern on a fourth semiconductor
7 layer, wherein the first, second and third checking patterns
8 overlap to form a first rectangular frame, the fourth
9 checking pattern is surrounded by the first rectangular
10 frame, a first pair of parallel sides of the first
11 rectangular frame is formed by the first checking pattern,
12 and a second pair of parallel sides of the first rectangular
13 frame is formed by the second and third checking patterns;

14 measuring overlap accuracy between the fourth checking
15 pattern and the first checking pattern; and

16 measuring overlap accuracy between the fourth checking
17 pattern and the second and third checking patterns.

1 2. The method as claimed in claim 1, wherein the second
2 checking pattern comprises a pair of second parallel line-
3 shaped patterns inside the second pair of parallel sides of
4 the first rectangular frame respectively.

1 3. The method as claimed in claim 2, wherein the third
2 checking pattern comprises a pair of third parallel line-
3 shaped patterns outside the second pair of parallel sides of
4 the first rectangular frame respectively.

1 4. The method as claimed in claim 1, wherein the fourth
2 checking pattern comprises a fourth line-shaped pattern to
3 form a second rectangular frame.

1 5. The method as claimed in claim 1, wherein the first
2 checking pattern comprises two pairs of first line-shaped
3 patterns on the first pair of parallel sides of the first

4 rectangular frame respectively and the two pairs of first
5 line-shaped patterns are parallel.

1 6. The method as claimed in claim 1, wherein the first
2 checking pattern comprises a pair of first parallel line-
3 shaped patterns on the first pair of parallel sides of the
4 first rectangular frame respectively.

1 7. The method as claimed in claim 1, further comprising:
2 measuring the first checking pattern to obtain a first
3 position in a first dimension;

4 measuring the fourth checking pattern to obtain a second
5 position in the first dimension; and

6 checking if the first and second positions fall within a
7 predetermined error range.

1 8. The method as claimed in claim 3, further comprising:
2 measuring the second and third line-shaped patterns on
3 one side of the second pair of parallel sides of the first
4 rectangular frame to obtain a first average position;

5 measuring the second and third line-shaped patterns on
6 the other side of the second pair of parallel sides of the
7 first rectangular frame to obtain a second average position;

8 averaging the first average position and the second
9 average position to obtain a third position;

10 overlap scanning the fourth checking pattern on the
11 fourth semiconductor layer to obtain a fourth position of the
12 fourth checking pattern along the direction parallel to the
13 first pair of parallel sides; and

14 checking if the third and fourth positions fall within a
15 predetermined error range.

1 9. The method as claimed in claim 1, wherein the second
2 checking pattern comprises a second line-shaped pattern on
3 one side of the second pair of parallel sides of the first
4 rectangular frame and the third checking pattern comprises a

5 third line-shaped pattern on the other side of the second
6 pair of parallel sides of the first rectangular frame.

1 10. The method as claimed in claim 9, further comprising:
2 measuring the second line-shaped pattern on one side of
3 the second pair of parallel sides of the first rectangular
4 frame to obtain a first position X'01 of the second line-
5 shaped pattern;

6 measuring the third line-shaped pattern on the other side
7 of the second pair of parallel sides of the first rectangular
8 frame to obtain a second position X'02 of the third line-
9 shaped pattern;

10 averaging the first position X'01 of the second line-
11 shaped pattern and the second position X'02 of the third
12 line-shaped pattern to obtain a third position representing
13 the average location of the second and third checking
14 patterns;

15 overlap scanning the fourth checking pattern along the
16 direction parallel to the first pair of parallel sides of the
17 first rectangular frame to obtain a fourth position; and

18 checking if the third and fourth positions fall within a
19 predetermined error range.

1 11. A method of checking overlap accuracy of patterns on
2 four stacked semiconductor layers, comprising:

3 forming a first checking pattern on a first semiconductor
4 layer, a second checking pattern on a second semiconductor
5 layer, a third checking pattern on a third semiconductor
6 layer and a fourth checking pattern on a fourth semiconductor
7 layer, wherein the first, second and third checking patterns
8 overlap to form a first rectangular frame, a first pair of
9 parallel sides of the first rectangular frame is formed by
10 the first checking pattern, a second pair of parallel sides
11 of the first rectangular frame is formed by the second and

12 third checking patterns, and the fourth checking pattern is
13 arrayed as a second rectangular frame and is surrounded by
14 the first rectangular frame;

15 measuring overlap accuracy between the fourth checking
16 pattern and the first checking pattern; and

17 measuring overlap accuracy between the fourth checking
18 pattern and the second and third checking patterns.

1 12. The method as claimed in claim 11, wherein the second
2 checking pattern comprises a pair of second parallel line-
3 shaped patterns inside the second pair of parallel sides of
4 the first rectangular frame respectively.

1 13. The method as claimed in claim 12, wherein the third
2 checking pattern comprises a pair of third parallel line-
3 shaped patterns outside the second pair of parallel sides of
4 the first rectangular frame respectively.

1 14. The method as claimed in claim 11, wherein the second
2 checking pattern comprises a second line-shaped pattern on
3 one side of the second pair of parallel sides of the first
4 rectangular frame, and the third checking pattern comprises a
5 third line-shaped pattern on the other side of the second
6 pair of parallel sides of the first rectangular frame.

1 15. The method as claimed in claim 11, wherein the first
2 checking pattern comprises two pairs of first line-shaped
3 patterns on the first pair of parallel sides of the first
4 rectangular frame respectively and the two pairs of first
5 line-shaped patterns are parallel.

1 16. The method as claimed in claim 11, wherein the first
2 checking pattern comprises a pair of first parallel line-
3 shaped patterns on the first pair of parallel sides of the
4 first rectangular frame respectively.

1 17. The method as claimed in claim 11, further
2 comprising:

3 measuring the first checking pattern to obtain a first
4 position in a first dimension;
5 measuring the fourth checking pattern to obtain a second
6 position in the first dimension; and
7 checking if the first and second positions fall within a
8 predetermined error range.

1 18. The method as claimed in claim 13, further
2 comprising:

3 measuring the second and third line-shaped patterns on
4 one side of the second pair of parallel sides of the first
5 rectangular frame to obtain a first average position;

6 measuring the second and third line-shaped patterns on
7 the other side of the second pair of parallel sides of the
8 first rectangular frame to obtain a second average position;

9 averaging the first average position and the second
10 average position to obtain a third position;

11 overlap scanning the fourth checking pattern on the
12 fourth semiconductor layer to obtain a fourth position of the
13 fourth checking pattern along the direction parallel to the
14 first pair of parallel sides; and

15 checking if the third and fourth positions fall within a
16 predetermined error range.

1 19. The method as claimed in claim 14, further
2 comprising:

3 measuring the second line-shaped pattern on one side of
4 the second pair of parallel sides of the first rectangular
5 frame to obtain a first position X'01 of the second line-
6 shaped pattern;

7 measuring the third line-shaped pattern on the other side
8 of the second pair of parallel sides of the first rectangular
9 frame to obtain a second position X'02 of the third line-
10 shaped pattern;

11 averaging the first position X'01 of the second line-
12 shaped pattern and the second position X'02 of the third
13 line-shaped pattern to obtain a third position representing
14 the average location of the second and third checking
15 patterns;
16 overlap scanning the fourth checking pattern along the
17 direction parallel to the first pair of parallel sides of the
18 first rectangular frame to obtain a fourth position; and
19 checking if the third and fourth positions fall within a
20 predetermined error range.

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